Silicon Labs Introduces Industry's Broadest Portfolio for 56G/112G SerDes Clocking

-- Si539x Clocks Boost Lead in Frequency Flexibility and Jitter Performance --
-- Si56x Ultra Series™ XO/VCXOs Provide Any Frequency up to 3 GHz --

AUSTIN, Texas, June 25, 2018 /PRNewswire/ -- Silicon Labs (NASDAQ: SLAB) has expanded its timing portfolio to meet the high-performance clocking requirements of 56G PAM-4 SerDes and emerging 112G serial applications. With this portfolio expansion, Silicon Labs is the only timing supplier to offer a comprehensive selection of clock generators, jitter attenuating clocks, voltage-controlled crystal oscillators (VCXOs) and XOs for 100/200/400/600G designs that satisfy sub-100 fs reference clock jitter requirements with margin.

Leading manufacturers of switch SoCs, PHYs, FPGAs and ASICs, including Broadcom, Inphi, Intel, MACOM, Marvell, MediaTek and Xilinx, are migrating to 56G PAM-4 SerDes technology to support higher bandwidth 100G+ Ethernet and optical networking designs. To meet the stringent requirements of 56G SerDes reference clocks, hardware developers often require clocks with sub-100 fs (typical) RMS phase jitter specifications. These designs typically use a mix of other frequencies for CPU and system clocks. Silicon Labs is the first timing supplier to provide fully integrated clock IC solutions for 56G designs that integrate SerDes, CPU and system clocks into a single device.

In 56G applications, hardware developers often seek complete clock tree solutions guaranteeing sub-100 fs RMS phase jitter to ensure sufficient margin and de-risk product development. Silicon Labs' new clock and oscillator products meet these stringent 56G SerDes requirements today, as well as the needs of emerging 112G serial SerDes designs that will ramp in data center and communications applications in the future.

"Silicon Labs' new clock generators, jitter attenuators and VCXO/XOs comprise the industry's broadest portfolio of frequency-flexible, ultra-low-jitter timing devices for the latest 56G SerDes-based 100/200/400/600G communications and data center designs," said James Wilson, Senior Marketing Director for Silicon Labs' timing products. "Whether our customers are designing synchronous or free-running systems, we offer the right ultra-high-performance timing solutions to meet their 56G SerDes application needs."

Silicon Labs' Si5391 is the industry's lowest jitter, any-frequency clock generator. It is the only clock generator on the market that can provide all clock frequencies needed in 200/400/600G designs from a single IC while delivering sub-100 fs RMS phase jitter performance for 56G SerDes reference clocks. Featuring up to 12 differential outputs, the Si5391 clock is available in frequency flexible A/B/C/D grade options. A Precision Calibration P-grade option optimizes RMS phase jitter performance with a 69 fs (typical) specification for the primary frequencies needed in 56G SerDes designs. The Si5391 is a true sub-100 fs "clock tree on a chip" solution designed to synthesize all output frequencies from the same IC while meeting 56G PAM-4 reference clock jitter requirements with margin.

Silicon Labs' Si539x jitter attenuators lead the industry in jitter performance and frequency flexibility. Designed to meet the exacting specifications and high-performance requirements of Internet infrastructure, these ultra-low jitter clocks reduce cost and complexity for a wide range of timing applications. Si539x any-frequency jitter attenuating clocks generate any combination of output frequencies from any input frequency while delivering industry-leading jitter performance (90 fs RMS phase jitter). Si5395/4/2 P-grade devices offer best-in-class jitter (69 fs RMS typical phase jitter) for 56G/112G SerDes clocking applications.

The new Si56x Ultra Series VCXO and XO family is ideal for next-generation high-performance timing applications requiring ultra-low jitter oscillators. Si56x VCXO/XOs are customizable to any frequency up to 3 GHz, supporting twice the operating frequency range of previous Silicon Labs VCXO products with half the jitter. The Si56x oscillators are available with single, dual, quad, and I2C-programmable options in industry-standard 5 mm x 7 mm and 3.2 mm x 5 mm packages, enabling drop-in compatibility with traditional XO, VCXOs and VCSOs. This family features devices with typical phase jitter as low as 90 fs.

Silicon Labs also offers the Si54x Ultra Series XO family for applications requiring tighter stability and guaranteed long-term reliability, such as optical transport networking (OTN), broadband equipment, data centers and industrial systems. The Si54x XOs are purpose-built for 56G designs, which rely on four-level pulse-amplitude modulation (PAM-4) signaling for serial data transmission to increase the bit rate per channel while keeping the bandwidth constant. Using an Si54x XO as a low-jitter reference clock maximizes signal-to-noise ratio (SNR) headroom, minimizes bit errors and enhances signal integrity. The Si54x family offers best-in-class performance, with typical phase jitter as low as 80 fs.

Pricing and Availability
Samples and production quantities of Silicon Labs' new clocks and Ultra Series oscillators are available now. These timing products are priced (USD) in 10,000-unit quantities as follows:

- Si5391 clock generator – from $6.05
- Si539x jitter attenuating clocks – from $6.60
- Si56x XO/VCXOs – from $5.21

Silicon Labs provides a wide range of evaluation boards (EVBs) to accelerate device evaluation and development. Clock and oscillator EVB pricing ranges from $95 to $299 (USD MSRP). The Si5391 and Si539x families are supported by Silicon Labs' ClockBuilder Pro (CBPro) software, which makes device configuration and customization easy. Customers can tailor a clock solution to their specific requirements using CBPro and receive samples as soon as two weeks.

To learn more about Silicon Labs' timing solutions for 56G applications and to order samples and evaluation boards for the Si5391 clock generator, Si539x jitter attenuators and Si56x/4x XO/VCXOs, visit www.silabs.com/56G.

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