Industry's First Low-Power PCI Express Gen 4 Buffers Raise the Bar in Power and Performance

-- New Si532xx Buffer Family First to Deliver PCIe Gen 4-Compliant Solution for Low-Power 1.5 V/1.8 V Applications --

AUSTIN, Texas – March 14, 2018 – Silicon Labs (NASDAQ: SLAB) has introduced a new family of low-power PCI Express® (PCIe®) Gen 1/2/3/4 clock buffers that provide ultra-low jitter clock distribution in 1.5 V and 1.8 V applications. With additive jitter performance of 40 fs RMS (typical), Silicon Labs' new Si532xx PCIe clock buffers provide more than 90 percent margin to stringent PCIe Gen 3 and Gen 4 jitter specifications, simplifying clock distribution and de-risking product development.

Increasingly, data center hardware designs including network interface cards (NICs), PCIe bus expanders and high-performance computing (HPC) accelerators are using low-power 1.5 V or 1.8 V supplies to minimize overall power consumption. Powered from a single 1.5 V-1.8 V supply and featuring up to 12 clock outputs, the Si532xx buffers are ideally suited to provide low-jitter PCIe clock distribution in low-power designs. The Si532xx clocks support PCIe Common Clock, Separate Reference No Spread (SRNS) and Separate Reference Independent Spread (SRIS) architectures, enabling them to be used in a wide variety of applications.

The Si532xx clocks are non-PLL-based fan out buffers, supporting the distribution of spread spectrum clock signals without impacting signal integrity. As the number of PCIe endpoints continues to expand in server and storage applications, system designers are tasked with buffering more copies of the PCIe reference clock. The new Si532xx family's ultra-low jitter performance enables designers to cascade multiple buffers while still meeting the maximum allowable system PCIe jitter budget of 0.5 ps RMS.

The Si532xx device output drivers leverage Silicon Labs' push-pull HCSL technology, which eliminates the need for external termination resistors required by conventional PCIe buffers using constant-current output driver technology. Internal power filtering prevents power supply noise from degrading clock jitter performance, eliminating discrete low-dropout regulators required by competing solutions. The Si532xx family supports both 85 ohm and 100 ohm impedance options.

"We've leveraged Silicon Labs' expertise in high-performance clock design to reduce jitter and power consumption in PCIe clock distribution applications," said James Wilson, Senior Marketing Director for Silicon Labs' timing products. "Our new Si532xx family demonstrates Silicon Labs' commitment to help consolidate and simplify high-speed clock tree designs in data center, industrial, communications and consumer designs."

Because clock jitter is a critical design parameter for all PCIe applications, Silicon Labs offers PCIe Gen 1/2/3/4 software that simplifies PCIe jitter measurements. This easy-to-use utility is available for developers to download from www.silabs.com/pcie-learningcenter.

Pricing and Availability

Samples and production quantities of the Si532xx PCIe clock buffers are available now in multiple output options. The Si53212, Si53208 and Si53204 clocks provide twelve, eight and four PCIe clock outputs. Samples ship in two weeks, and production quantities are available in four weeks. Pricing in 10,000-unit quantities ranges from $1.40 (USD) for the 4-output device to $2.17 (USD) for the 12-output clock. Silicon Labs' new Si53204-EVB development kit, priced at $175 (USD MSRP), provides quick, simple PCIe buffer evaluation. For more information about the Si532xx PCIe buffer family or to order samples and development kits, visit www.silabs.com/clock-buffers.

Silicon Labs

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