PCI Express Gen 4 Clocks from Silicon Labs Set New Performance Standard for Data Center and Consumer Designs

-- New Si522xx PCIe Clock Family Delivers Industry-Leading Jitter Performance, Power Efficiency and Single-Chip Integration --

AUSTIN, Texas – Sept. 27, 2017 – Silicon Labs (NASDAQ: SLAB) today introduced a family of clock generators providing the industry's lowest jitter, highest integration and lowest power consumption for applications using PCI Express® (PCIe®) Gen 1/2/3/4. Silicon Labs' new Si522xx PCIe clock generators meet the stringent requirements of PCIe Gen 4 with 20 percent jitter margin while providing 60 percent margin to PCIe Gen 3 jitter specifications. Developers can now design PCIe-compliant solutions with confidence knowing Silicon Labs' PCIe clocks maximize jitter margin and de-risk product development.

Featuring PCIe Gen 4 compliance and up to 12 clock outputs, the Si522xx clocks are ideally suited to provide low-jitter PCIe clock generation and distribution in data center applications, eliminating the need for standalone clock buffers. In addition to providing best-in-class jitter margin, the Si522xx clocks are fully compliant with PCIe Gen 4 Common Clock and Separate Reference Independent Spread (SRIS) architectures.

The Si522xx device output drivers leverage Silicon Labs' innovative push-pull HCSL technology, which eliminates the need for external termination resistors required by conventional PCIe clocks using constant-current output driver technology. Internal power filtering prevents power supply noise from degrading clock jitter performance, reduces component count and cuts board space by 30 percent compared to competing solutions.

Developers designing battery-powered applications like digital cameras are especially concerned about power consumption. The 2-output Si52202 clock is optimized for low-power 1.5 to 1.8 V applications, offering the industry's lowest power consumption for PCIe applications. Packaged in a small form factor 3 mm x 3 mm 20-QFN, the device is 45 percent smaller than competing solutions.

"Silicon Labs continues to drive innovation, performance and integration for PCI Express clocks," said James Wilson, Senior Marketing Director for Silicon Labs' timing products. "With the introduction of the Si522xx family, we are now able to serve the clocking needs for the entire universe of PCIe applications, from servers and storage to industrial and consumer applications."

Because clock jitter is a critical design parameter for all PCIe applications, Silicon Labs offers a free PCIe Gen 1/2/3/4 jitter measurement tool to developers at www.silabs.com/pcie-learningcenter.

Pricing and Availability

Samples and production quantities of the Si522xx PCIe clock generators are available now in multiple output options. The Si52212, Si52208 and Si52204 clocks provide 12, eight and four 100 MHz PCIe clock outputs with one 25 MHz LVCMOS reference. The Si52202 clock supports two 100 MHz outputs. Samples ship in two weeks, and production quantities are available in four weeks.

Pricing in 10,000-unit quantities starts from $1.27 (USD) for the 2-output device to $2.76 (USD) for the 12-output clock. Silicon Labs' new Si52204-EVB development kit, priced at $140 (USD MSRP) provides quick, simple PCIe clock evaluation. For more information about the Si522xx PCIe clock family or to order samples and development kits, visit www.silabs.com/pcie-clocks.

Silicon Labs

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