Silicon Labs Launches Industry's First Wireless Clocks Supporting 4G/LTE and Ethernet

-- New Si5381/82/86 Timing Devices Replace Multiple Clock ICs and VCXOs in Radio Access Networks --

AUSTIN, Texas, Sept. 25, 2017 /PRNewswire/ -- Silicon Labs (NASDAQ: SLAB) has introduced a new family of high-performance, multi-channel jitter attenuating clocks for 4.5G and Ethernet-based Common Public Radio Interface (eCPRI) wireless applications. The new Si5381/82/86 clocks leverage Silicon Labs' proven DSPLL technology to deliver an advanced timing solution that combines 4G/LTE and Ethernet clocking in a single IC. These highly integrated clocks eliminate the need for multiple clock devices and voltage-controlled crystal oscillators (VCXOs) in demanding applications including small cells, distributed antenna systems (DAS), m-BTS, baseband units (BBU) and fronthaul/backhaul equipment.

Over the next several years, service providers will lay the groundwork for 5G by deploying small cells, pico cells, DAS, µ-BTS and backhaul equipment that complements existing 4G/LTE networks by increasing outdoor network coverage and capacity and improving indoor signal reception. As carriers transition to Ethernet-based eCPRI fronthaul networks to increase the capacity of fronthaul connections between baseband units and remote radio heads, they are also deploying heterogeneous network (HetNet) equipment at the edge of the network where cost, power and size constraints present unique challenges for hardware designers. By combining 4G/LTE and Ethernet clocking in a single IC, the Si538x family dramatically simplifies HetNet clock generation, providing a breakthrough solution that is 55 percent lower power and 70 percent smaller than competing solutions.

"HetNet and eCPRI equipment deployments are paving the way to 5G. By choosing Silicon Labs' Si538x wireless clocks, wireless system designers can minimize the cost, power and complexity of small cells, DAS, m-BTS and other designs," said James Wilson, Senior Marketing Director for Silicon Labs' timing products. "Silicon Labs' DSPLL-based Si538x clocks are the industry's first timing ICs that combine low-phase-noise 4G/LTE clocking and low-jitter Ethernet clocking in the same device. We're excited to see wireless customers adopting our technology to optimize HetNet designs and accelerate the deployment of 4.5G networks."

The Si538x clocks are optimized to provide reference timing for HetNet equipment. Small cells and DAS equipment are "all-in-one" base stations that need reference timing for 4G/LTE transceivers, baseband processing and Ethernet/Wi-Fi connectivity. The Si5386 clock's low-phase-noise DSPLL replaces a discrete clock IC, VCXO and loop filter components in a compact, single-chip design. In addition, the Si5386 clock integrates five MultiSynth fractional clock synthesizers to provide simplified Ethernet and baseband reference timing. This streamlined, single-PLL + MultiSynth architecture provides superior reliability to alternate solutions that rely on multiple PLLs and discrete oscillators.

Baseband units have complex timing requirements requiring multiple independent clock domains for CPRI links to remote radio heads, Ethernet-based fronthaul networks (including eCPRI) and general-purpose clocks for local baseband processing. The Si5381/82 clocks combine a high-speed, low-phase-noise DSPLL supporting wireless frequencies up to 3 GHz with flexible any-rate DSPLLs optimized for Ethernet and general-purpose timing. Like the Si5386 clock, the Si5381/82 devices require no external VCXOs or crystals. All PLL components are integrated on-chip in a space-saving 9 mm x 9 mm 64-LGA package. In addition, the Si538x clocks support a hitless switching capability that enables system designers to easily switch between different clock inputs and minimize output clock phase transients, ensuring downstream PLLs remain in lock.

Like other clock products from Silicon Labs, the Si538x devices are configurable and customizable using Silicon Labs' flexible ClockBuilder Pro software.

Pricing and Availability
Samples of the Si5381/82/86 wireless clocks are available now, and production quantities are planned to be available in December. Samples ship in two weeks, and production quantities are available in four weeks. Pricing in 10,000-unit quantities starts from $6.77 (USD) for the Si5386 clock. Silicon Labs' new Si5381E-E-EVB, Si5382E-E-EVB and Si5386E-E-EVB development kits, priced at $299 each (USD MSRP), provide quick, simple device evaluation. For more information about the Si5381/82/86 clock family or to order samples and development kits, visit www.silabs.com/wireless-jitter-attenuators.

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Connect with Silicon Labs
Silicon Labs PR Contact: Dale Weisman +1-512-532-5871, dale.weisman@silabs.com

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