# PCI Express Clock Jitter Measurement Tool from Silicon Labs Simplifies Timing Design

### Free, Easy-to-Use Software Takes the Guesswork out of PCI Express Development

*“As part of our vision of simplifying timing design, we developed the clock jitter tool to make the task of obtaining PCIe jitter measurements as fast, easy and accurate as possible”*

AUSTIN, Texas--(BUSINESS WIRE)--Silicon Labs (NASDAQ: SLAB) has introduced a free software tool that enables engineers to quickly and easily measure PCI Express® (PCIe®) clock jitter from an oscilloscope data file in just a few simple clicks, making it easy to verify PCIe specification compliance and reduce system development time. Silicon Labs’ clock jitter tool is the first standardized jitter calculator readily available for the PCIe 1.0, 2.0, 3.0 and 4.0 specifications, at no charge, to anyone developing applications based on the popular PCIe architecture. Designed to support PCIe common clock and separate clock architectures, the tool is open to the industry and not restricted for use with Silicon Labs’ clock products.

Silicon Labs’ jitter measurement tool for PCIe technology is available to developers now and can be downloaded free of charge at www.silabs.com/pcie-learningcenter.

Since its inception as a serial interconnect for desktop PCs more than a decade ago, the PCIe standard has evolved over three generations to become widely deployed in blade servers, storage, embedded computing, IP gateways, industrial systems and consumer electronics. PCIe technology has also been adopted for FPGA and SoC devices to provide a versatile, high-performance means of transferring data within systems. While the PCIe specification specifies a 100 MHz reference clock with ±300 ppm frequency stability, some FPGA and SoC designs may operate internally up to 250 MHz, making clock jitter evaluation a critical design consideration.

Filter masks and jitter calculations for PCIe technology are often misunderstood during the development process. Most oscilloscopes are not equipped with the necessary filter masks to enable correct PCIe clock jitter measurements, which can lead to confusion regarding why a measured result does not match data sheet specifications. Developers often report PCIe jitter measurements higher than clock data sheet specifications, indicating incorrect measurements rather than design issues. As a leading supplier of PCIe clock products, Silicon Labs created the PCIe jitter tool to address these needs, providing hardware designers with a downloadable utility that quickly determines if the measured clock meets PCIe jitter requirements.

Silicon Labs’ clock jitter tool for PCIe technology features an intuitive graphical user interface that guides developers through the few simple steps required to compute clock jitter from an oscilloscope data file. The tool includes all filter masks defined by the PCI-SIG® for PCIe 1.0, 2.0, 3.0 and 4.0 common clock and separate reference clock architectures, supporting both independent spread spectrum (SRIS) and non-spread spectrum (SRNS) technologies. The jitter results are displayed in a concise, easy-to-read summary format that takes the guesswork out of ensuring the system design meets PCIe specifications with sufficient jitter margin. For added convenience, the jitter measurements can be saved as a PDF file for future reference.

In related news, Silicon Labs has announced that its clock generators and buffers for PCIe applications meet PCIe 4.0 specification requirements. All associated product datasheets have been updated to reflect agreement with the PCI Express Base Specification 4.0, rev 0.5.

“As part of our vision of simplifying timing design, we developed the clock jitter tool to make the task of obtaining PCIe jitter measurements as fast, easy and accurate as possible,” said James Wilson, director of marketing for Silicon Labs’ timing products. “As a service to the industry, we’ve made this helpful clock jitter calculator freely available to all developers working with the PCIe data bus standard, regardless of the clock IC vendor they are using.”

**About Silicon Labs’ Timing Products**

Silicon Labs offers a comprehensive portfolio of timing devices including crystal oscillators (XOs), voltage-controlled crystal oscillators (VCXOs), any-frequency, any-output clock generators, clock buffers, jitter attenuators, network synchronizers, and PCIe Gen 1/2/3/4 clock generators and buffers. Leveraging patented DSPLL and MultiSynth technologies, Silicon Labs’ timing products provide best-in-class jitter performance, frequency flexibility and integration, minimizing the bill-of-materials (BOM) cost and complexity associated with clock generation and distribution. To help developers get to market faster, Silicon Labs offers a wide range of easy-to-use tools, fast and easy customization, and short, two-week lead times for samples – even for custom-configured products. For more information, please visit www.silabs.com/timing.

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