Silicon Labs Announces Industry's First Single-Chip Clock IC for Wireless Base Stations

Ultra-Low Phase Noise Si5380 Clock IC Reduces BOM Cost, Footprint and Power in Small Cell and Macro Cell Applications

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AUSTIN, Texas--(BUSINESS WIRE)--Silicon Labs (NASDAQ: SLAB), a leading provider of high-performance timing solutions for Internet infrastructure, today introduced the industry's most highly integrated clock IC for wireless infrastructure applications including small cell and macro cell base stations. Silicon Labs' new Si5380 clock generator is the industry's first clock IC capable of replacing a low phase noise integer-N clock, voltage-controlled crystal oscillator (VCXO), discrete loop filters and voltage regulator components with one single-chip device. The Si5380 clock provides comparable phase noise performance to discrete conventional solutions while delivering breakthrough advancements in solution footprint, bill of materials (BOM) cost, power consumption, performance and ease of use.

According to a recent Cisco study, global mobile data traffic will soar nearly ten-fold between 2014 and 2019, driven by video streaming services and the widespread adoption of IoT-connected devices. While base station suppliers are tasked with developing new 4G/LTE equipment that increases network capacity and coverage, it is becoming an increasingly difficult design challenge for small cells because they are often deployed in space-constrained, low-power outdoor locations in congested urban environments. Silicon Labs' new Si5380 clock is the industry's first single-chip wireless clock IC optimized for size, power, integration and performance, making it an ideal fit for small cell applications.

The Si5380 clock leverages Silicon Labs' latest fourth-generationDSPLL technology to provide a purpose-built solution optimized for next-generation small cells and macro cell remote radio head (RRH) designs. DSPLL technology's innovative dual-loop mixed-signal architecture integrates a single high-performance 15 GHz analog voltage-controlled oscillator within a digital phase-locked-loop (PLL) architecture that eliminates the need for discrete loop filters and low-drop-out (LDO) regulators. The resulting clock solution provides an optimal combination of ultra-low phase noise clock synthesis with best-in-class PLL integration.

The Si5380 clock has a 66 percent smaller printed circuit board (PCB) footprint and 30 percent lower power consumption than competing VCXO-based clock IC solutions. Power-efficient timing components are especially important for today's small cells, which have limited power budgets and often are powered using Power over Ethernet (PoE) technology. Given that the DSPLL integrates all PLL and power supply regulation elements on-chip, the Si5380 device delivers high board-level noise immunity, integrated power supply noise rejection and consistent, repeatable phase noise performance across temperature.

While VCXO-based clock solutions often suffer from degraded spurious performance when subjected to vibration, the Si5380 device's integrated DSPLL technology provides excellent spurious response regardless of the system environment. Furthermore, the Si5380 clock guarantees low phase noise operation when locked to a high jitter input clock, ensuring that data converter performance is not degraded by external effects. The Si5380 generates 4G/LTE frequencies up to 1.47456 GHz and provides up to 12 independently configurable clocks, which can be used for clocking JESD204B-compliant data converters, FPGAs and other logic devices.

"The Si5380 clock is the industry's most integrated timing solution available for macro and small cell base stations requiring compact PCB footprints, low power consumption, and robust, carrier-grade phase noise performance across a wide range of environmental conditions," said James Wilson, marketing director for Silicon Labs' timing products. "The combination of Silicon Labs' highly integrated DSPLL-based clock architecture and easy-to-use ClockBuilder Pro software greatly simplifies the challenges of clock synthesis and jitter attenuation for today's heterogeneous wireless networks."

Simplifying Clock Trees with ClockBuilder Pro

To simplify clock tree design for wireless base stations, Silicon Labs' ClockBuilder Pro software enables designers to generate programmable Si5380 clock configurations in less than five minutes, minimizing software development overhead. Instead of waiting months for custom clock devices, designers simply upload their custom configurations to Silicon Labs through ClockBuilder Pro. Factory pre-programmed Si5380 clock samples ship in two weeks, accelerating the overall product development process with the industry's shortest custom sample lead times.

Pricing and Availability

Factory pre-programmed samples and production quantities of the Si5380 clock are available now. Product pricing in 10,000-unit quantities begins at less than $6 (USD). The Si5380-EVB evaluation board, available now and priced at $399 (USD MSRP), enables developers to move quickly from device configuration to detailed performance evaluation. ClockBuilder Pro software is available from Silicon Labs' website at no charge. For more information about Silicon Labs' Si5380 ultra-low phase noise clock generator, to order samples and evaluation boards, and to download ClockBuilder Pro, visit www.silabs.com/clocks.

Silicon Labs

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