Silicon Labs Simplifies Clock Tree Design for Complex Internet Infrastructure Applications

Easy-to-Use Web-Based Utility Turns Embedded Developers into Timing Experts, Generating Custom Clock Tree Recommendations in Minutes

“ While growing demand for high-speed Internet infrastructure equipment is driving the complexity of timing architectures, we’re committed to making clock tree design as fast and easy as possible for developers ”

AUSTIN, Texas--(BUSINESS WIRE)--Silicon Labs (NASDAQ: SLAB), a leader in high-performance, analog-intensive, mixed-signal ICs, today launched an online timing utility that eases the complexity of designing clock trees for a wide range of Internet infrastructure applications including high-speed networking, telecommunications and data center equipment. Silicon Labs’ new Clock Tree Expert tool enables embedded developers to generate sophisticated, streamlined clock tree block diagrams within minutes, simplifying system design, reducing bill of materials (BOM) count and speeding time to market.

Today’s networking and telecom equipment designers are under pressure to deliver best-in-class products at competitive prices. Timing component selection and clock tree design are more important than ever because timing ICs provide low-jitter timing references for high-speed 10/40/100G data applications and can greatly impact system-level performance. When specifying clock trees for their applications, hardware designers must ensure critical jitter performance parameters are met with sufficient margin with the minimum number of timing components. Choosing the optimal combination of clocks, oscillators, jitter attenuators and buffers can be a daunting and time-consuming task for a given Internet infrastructure application.

As a one-stop shop supplier of timing products with industry-leading technology, Silicon Labs is committed to providing the tools needed to simplify component selection and clock tree development. Leveraging Silicon Labs’ DSPLL and MultiSynth technologies, the web-based Clock Tree Expert tool frees developers from the burden of designing clock trees by recommending the optimal combination of highly integrated, low-jitter, frequency-flexible clocks and oscillators required to consolidate timing BOM into the fewest number of components.

The Clock Tree Expert is intuitive and easy to use. Users simply enter the required frequencies, number of clocks and desired signaling format, and the tool generates a recommended clock tree in seconds using the minimum number of timing components. Experienced users can also use the tool’s “Build Your Own” environment to design clock trees to their exact specifications. The Clock Tree Expert then guides the user to find the optimal timing ICs, save and share clock tree designs, generate a BOM list and order samples. When combined with industry-best lead times of less than two weeks, Silicon Labs’ timing tools significantly accelerate time to market.

In addition to streamlining clock tree design, the Clock Tree Expert provides instant access to Silicon Labs’ comprehensive timing product information and data sheets. Customize buttons automatically take developers to Silicon Labs’ suite of timing customization tools, which can be used to generate custom crystal oscillator (XO), voltage-controlled oscillator (VCXO), CMEMS® oscillator and CMOS/differential clock generator part numbers (www.silabs.com/custom-timing).

“While growing demand for high-speed Internet infrastructure equipment is driving the complexity of timing architectures, we’re committed to making clock tree design as fast and easy as possible for developers,” said James Wilson, director of marketing for Silicon Labs’ timing products. “Silicon Labs’ Clock Tree Expert tool makes embedded developers instant timing experts by automating the process of creating and customizing clock trees and accelerating the hardware development process. This productivity tool takes the guesswork out of component selection, making it easy to select the best combination of timing devices from Silicon Labs’ broad product portfolio.”

For more information and to access Silicon Labs’ complimentary Clock Tree Expert tool, please visit www.silabs.com/timing-tools.

About Silicon Labs’ Timing Products

Silicon Labs offers a comprehensive portfolio of timing devices including crystal oscillators, voltage-controlled oscillators, MEMS-based CMEMS oscillators, any-frequency, any-output clock generators, jitter attenuators, PCI Express clocks and clock buffers. Leveraging patented DSPLL and MultiSynth technologies, Silicon Labs’ timing ICs give designers the ultimate in frequency flexibility while still delivering the best jitter performance in the industry, minimizing board space and simplifying designs. To help developers get to market faster, Silicon Labs is committed to offering a wide range of easy-to-use tools, fast and easy customization, and short two-week lead times for samples – even for custom-configured products. For more information, please visit www.silabs.com/timing.

Silicon Labs

Silicon Labs is an industry leader in the innovation of high-performance, analog-intensive, mixed-signal ICs. Developed by a world-class engineering team with unsurpassed expertise in mixed-signal design, Silicon Labs' diverse portfolio of patented semiconductor solutions offers customers significant advantages in performance, size and power consumption. For more information about Silicon Labs, please visit www.silabs.com.

Cautionary Language

This press release may contain forward-looking statements based on Silicon Labs' current expectations. These forward-looking statements involve risks and uncertainties. A number of important factors could cause actual results to differ materially from those in the forward-looking statements. For a discussion of factors that could impact Silicon Labs' financial results and cause actual results to differ materially from those in the forward-looking statements, please refer to Silicon Labs' filings with the SEC. Silicon Labs disclaims any intention or obligation to update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

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