

Silicon Labs Launches Industry's Lowest Jitter Clock Family for Data Centers and Internet Infrastructure

Ultra-Frequency-Flexible Si534x "Clock-Tree-on-a-Chip" Family Features First Fractional Synthesis and Jitter Attenuation Clocks with <100 fs Jitter

"To keep pace with the accelerating complexity of Internet infrastructure, hardware developers need advanced timing solutions to simplify system design and speed time to market"

AUSTIN, Texas--([BUSINESS WIRE](#))--[Silicon Labs](#) (NASDAQ: SLAB), a leader in high-performance, analog-intensive, mixed-signal ICs, today introduced the industry's most frequency-flexible clock solutions offering industry-leading jitter performance for high-speed networking, communications and data center equipment serving as the foundation of today's [Internet infrastructure](#). Silicon Labs' next-generation Si534x "clock-tree-on-a-chip" portfolio includes high-performance clock generators and highly integrated multi-PLL jitter attenuators. These single-chip, ultra-low-jitter timing devices combine clock synthesis and jitter attenuation functionality to reduce the cost and complexity of optical networking, wireless infrastructure, broadband access/aggregation, Carrier Ethernet, test and measurement, and enterprise/data center equipment including edge routers, switches, storage and servers.

Skyrocketing demands for bandwidth and the growing complexity of Internet infrastructure and data center systems are driving the need for a wide variety of clocks at different frequencies, signaling formats and voltage levels. Jitter performance requirements to support the highest data rates for 10/40/100G networks are also very demanding. Given the limited flexibility and integration of traditional clock solutions, hardware designers are often forced to use a costly and complicated combination of clock generators, jitter attenuators, oscillators and buffers to complete their clock trees. To address this industry need, Silicon Labs' new Si534x jitter attenuators and clock generators leverage industry-leading frequency flexibility and clock-tree-on-a-chip integration to deliver an efficient, cost-effective solution that combines all discrete timing functions into a single-chip clock IC solution.

Silicon Labs' Si5347/46/45/44/42 jitter attenuators and Si5341/40 clock generators provide an I²C-configurable platform with an industry-leading combination of frequency translation capabilities and best-in-class jitter performance (<100 fs RMS). By combining up to four independent jitter-attenuating PLLs and up to five ultra-low-jitter [MultiSynth fractional synthesizers](#), the Si534x family is capable of generating up to 10 outputs with any combination of frequencies from 100 Hz to 800 MHz in a wide range of user-selectable output formats (LVPECL, LVDS, CML, HCSL and LVCMOS). This exceptional level of integration and frequency flexibility eliminates the need for multiple clock ICs, discrete level translation, loop filters and power supply filter components and significantly reduces bill of materials (BOM) cost and complexity while still providing more than 50 percent margin to stringent 10/40/100G jitter specifications.

Simplifying Clock Trees with ClockBuilder Pro

With Silicon Labs' Si534x family and new [ClockBuilder Pro](#) software, high-performance clock configuration has never been simpler or faster. ClockBuilder Pro is designed to help system designers quickly and easily create custom Si534x clocks for their applications. This easy-to-use software integrates the equivalent of more than 150 engineer-years of Silicon Labs' [DSPLL](#)® timing technology and applications expertise to simplify clock tree design and speed time to market. Using the intuitive ClockBuilder Pro GUI, designers can quickly generate sophisticated device configurations in less than five minutes, minimizing software development overhead.

Silicon Labs' complimentary ClockBuilder Go app for mobile devices simplifies the design process even further. System designers can quickly jumpstart their clock tree designs on their smartphones and tablets by leveraging Silicon Labs' built-in frequency planning algorithms to synthesize virtually any clock frequency. ClockBuilder Go is available today for iOS mobile devices, and Android support will be available later this year.

Rather than waiting months to receive their custom clock orders, system designers simply upload their custom configurations to Silicon Labs through ClockBuilder Pro software. Factory pre-programmed Si534x clock samples ship in two weeks, accelerating the overall product development process with the industry's shortest custom sample lead times.

“To keep pace with the accelerating complexity of Internet infrastructure, hardware developers need advanced timing solutions to simplify system design and speed time to market,” said Mark Thompson, vice president and general manager of Silicon Labs’ timing products. “The combination of Silicon Labs’ easy-to-use ClockBuilder Pro software and high-performance Si534x portfolio provides the best solution available today for clock synthesis and jitter attenuation, offering unsurpassed jitter performance and frequency flexibility for high data rate applications.”

Pricing and Availability

Factory pre-programmed samples of the Si534x clock generators and jitter attenuators are available now in QFN packages as small as 7 mm x 7 mm. Si5341/40 clock generator pricing in 10K quantities ranges from \$4.75 to \$10.60 (USD), and Si534x jitter attenuator 10K pricing ranges from \$6.00 to \$29.00 (USD). Silicon Labs’ Si534x family evaluation boards, priced at \$200 and \$250 (USD MSRP), enable developers to move quickly from device configuration to detailed performance analysis to custom part number generation in less than five minutes. ClockBuilder Pro software is available from Silicon Labs’ website at no charge. For more information about Silicon Labs’ Si534x family, to order samples and evaluation boards, and to download ClockBuilder Pro, visit www.silabs.com/timing.

Silicon Labs

Silicon Labs is an industry leader in the innovation of high-performance, analog-intensive, mixed-signal ICs. Developed by a world-class engineering team with unsurpassed expertise in mixed-signal design, Silicon Labs’ diverse portfolio of patented semiconductor solutions offers customers significant advantages in performance, size and power consumption. For more information about Silicon Labs, please visit www.silabs.com.

Cautionary Language

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Contact:

Silicon Labs
Dale Weisman, +1-512-532-5871
dale.weisman@silabs.com

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